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**Introduction**

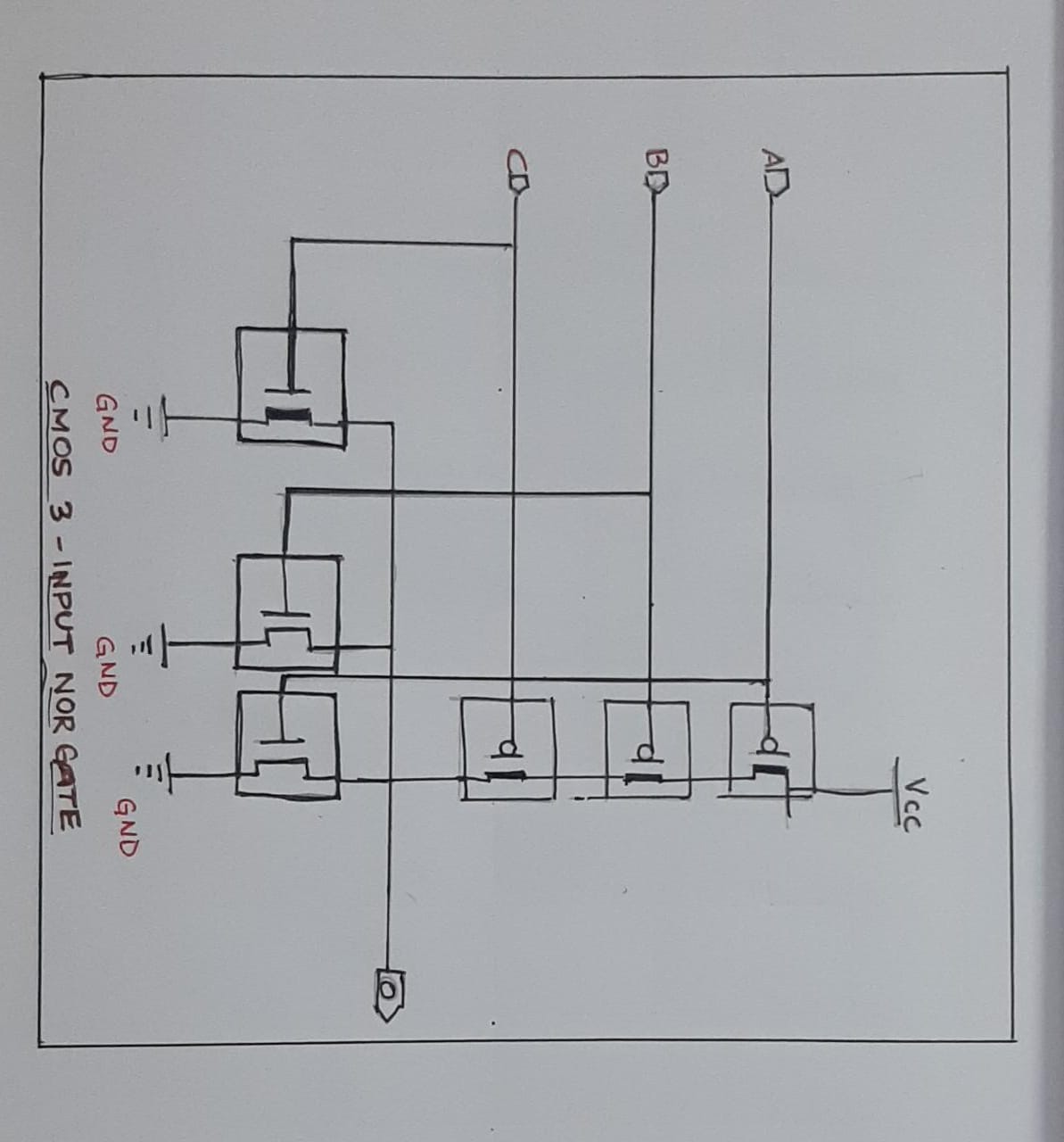
Basic gates such as inverter, NAND gate, and NOR gate are often utilized in the design of more sophisticated circuits with a higher number of transistors, such as SRAM cells, MUXs, ADCs, and other circuits. This repository presents the design and simulation of CMOS NOR gate using 28nm technology. Synopsis software has been used to build the design, which was then simulated in the PrimeWave environment.

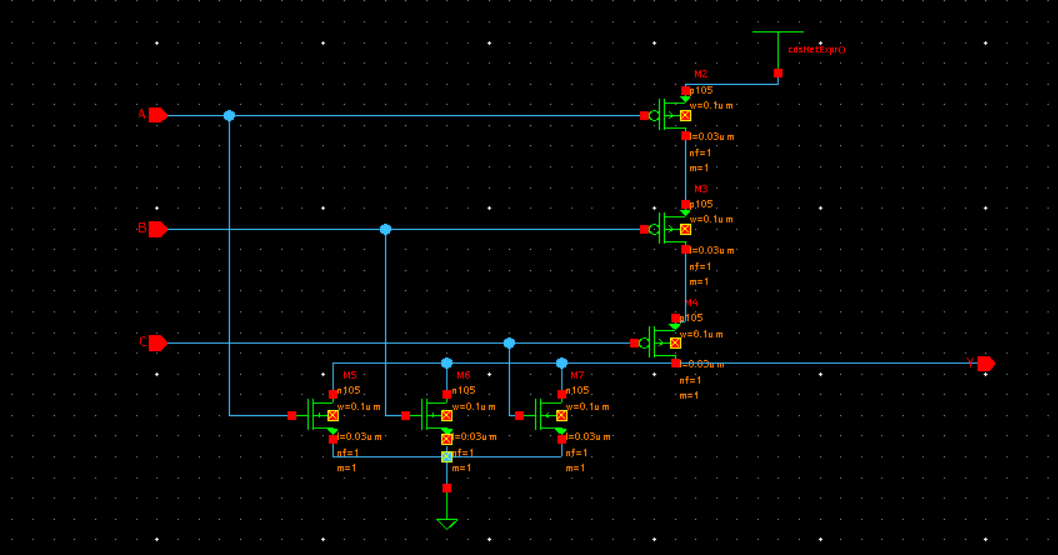
Device characterization

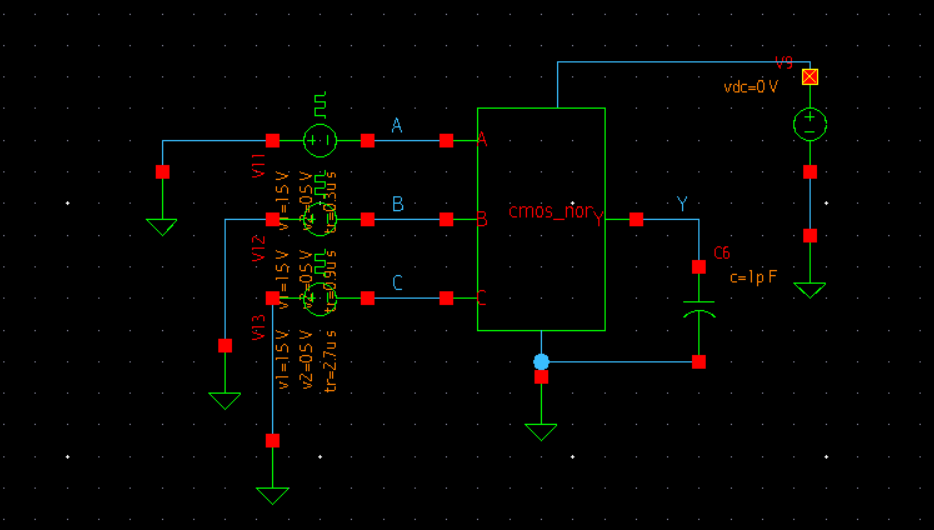
The three-input NOR3 gate uses three p-channel transistors asynchronous between Vdd and gate-output, and therefore the complementary circuit of a parallel-connection of three n-channel transistors are connected Ground and gate-output. In CMOS technology, N-type and P-type transistors are wont to design logic functions. the identical signal which activates a transistor of 1 type is employed to show OFF a transistor of the opposite type. This characteristic allows the planning of logic devices using only simple switches, without the necessity for a pull-up resistor. CMOS has high speed, low power dissipation, high noise margins within the two states, and can operate over a good range of source and input voltages. in a very CMOS NOR gate the output isn't left floating. This technology are often accustomed design analog circuits like image sensors, data converters, and microcontrollers..

**Circuit Design**

**REFERENCE CIRCUIT**

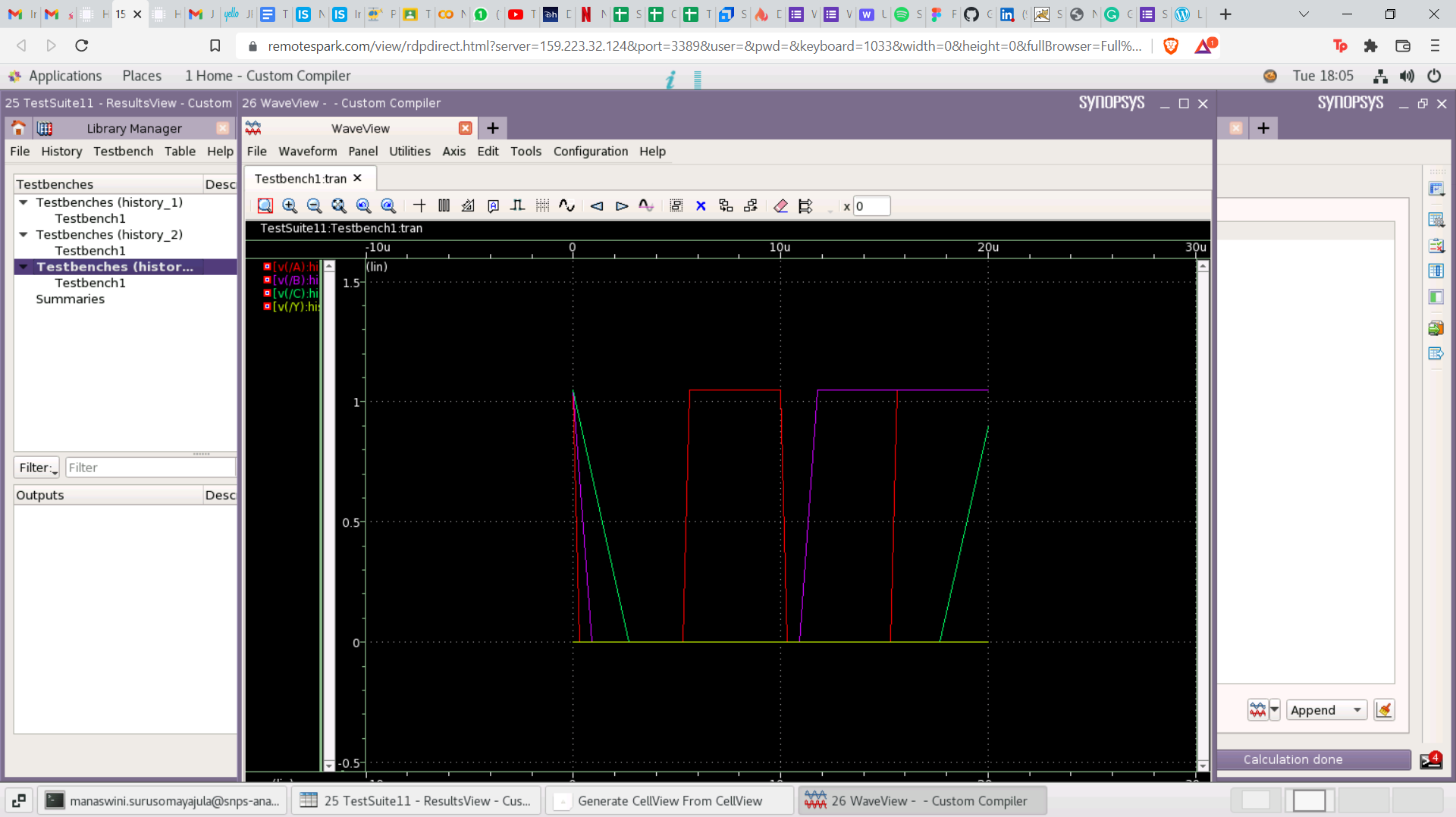


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**Simulation Results**

**WAVEFORM**

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**Conclusion**

1.This paper presents a CMOS NOR Gate.

2.Simulations using Synopsys' proprietary compiler in 28nm technology were used to verify the results.

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**Acknowledgements**

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KUNAL GHOSH,CO FOUNDER,VSD Corp.Pvt. Ltd.India

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2. Danny Rittman “28nm and below,New Path and Beyond”